What is claimed is:

1. A method of creating a hybridized chip using a top active optical device, having a substrate including a first side and active device contacts on the first side, the top active optical device also being on the first side, combined with an electronic chip having electronic chip contacts, when at least some of the active device contacts are not aligned with at least some of the electronic chip contacts, each of the at least some active device contacts having an electrically corresponding electronic chip contact, the method comprising:

creating sidewalls defining openings in the substrate, extending from the first side at the active device contacts to a bottom of the substrate opposite the first side, at points substantially coincident with the active device contacts;

making the sidewalls electrically conductive; and

connecting the points and the electronic chip contacts with an electrically conductive material.

2. The method of claim 1 wherein the making the sidewalls electrically conductive comprisies:

filling at least some of the openings with an electrically conductive material.

3. The method of claim 1 wherein the making the sidewalls electrically conductive comprises:

depositing an electrically conductive material on at least some of the sidewalls.

Sub B2

4. The method of claim 1 further comprising:

attaching a carrier to the top active optical device.

5. The method of claim 4 further comprising:

removing the carrier after connecting the points and the electronic chip contacts.

Sub A2

6. The method of claim 1 wherein the connecting comprises:

patterning traces between the points and the electronic chip contacts, and

making the traces electrically conductive.

7. The method of claim 6 wherein the patterning traces comprises:

patterning the traces on the substrate.

8. The method of claim 6 wherein the patterning traces comprises:

patterning the traces on the electronic chip.

Sub B4

9. The method of claim 1 further comprising:

thinning the substrate.

10. The method of claim 1 further comprising attaching a carrier having a thickness greater than a minimum lasing thickness over the top active device.

11. The method of claim 10 further comprising:

patterning access ways in the carrier and applying an anti-reflection coating to the carrier.

12. A hybridized chip comprising:

at least one top active optical device coupled to an electronic chip, the hybridized chip having been created using the method of one of claims 1-11.

13. A method of connecting two chips, one of which being a topside active chip, each of the two chips having electrically corresponding contacts to be joined together that are physically mismatched relative to each other, the method comprising:

creating electrically conductive paths on an insulator, each of the electrically conductive paths extending between physical locations of contacts of one of the two chips and physical locations of the electrically corresponding contacts on the other of the two chips.

14. The method of claim 13 wherein the insulator has holes defined by sidewalls, and the creating the electrically conductive paths comprises:

making the holes electrically conductive.

15. The method of claim 14 wherein the making the holes electrically conductive comprises:

filling the holes with an electrically conductive material.

16. The method of claim 14 wherein the making the holes electrically conductive comprises:

depositing an electrically conductive material on the sidewalls.

17. The method of claim 13, wherein the insulator is part of one of the two chips, the method further comprising:

joining the other of the two chips to the insulator.

18. The method of claim 13, wherein the insulator is part of neither of the two chips, the method further comprising:

joining both of the two chips to the insulator.

19. A module comprising:

two chips connected together according to the method of one of claims 13-18